REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 19-22 are presently active; Claims 1-13 having been previously canceled, Claims 14-18 having been presently canceled without prejudice, and Claims 19-22 having been added by way of the present amendment. No new matter has been added.

In the outstanding Office Action, Claims 17-18 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claims 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lattimore et al (U.S. Pat. No. 5,831,896) in view of Rapp (U.S. Pat. No. 4,189,785).

Regarding the 35 U.S.C. § 112, first paragraph, rejection, the new claims have the subject matter that the voltage of the source terminal of the N-type MOS transistor of the second CMOS inverter circuit is switched at a "1" data writing time, and do not recite a second voltage (VSS – ΔV). Thus, it is respectfully submitted that the 35 U.S.C. § 112, first paragraph, rejection has been overcome.

According to the present invention recited in the new claims, as shown by way of the non-limiting examples in Figures 8 and 9, 5-transistor static random access memory (SRAM) cells 11 include first and second complementary metal oxide semiconductor (CMOS) inverter circuits 21 and 22 having a latch structure 12 and a control transistor 13, wherein when "1" data is written, at least an input threshold value (driver voltage) applied to the second CMOS inverter circuit 22 is changed temporarily. With this structure, a stable "1" data writing is enabled without losing a cell data area reduction effect, decreasing write speed or compromising stability. That is, in a semiconductor memory device having a memory structure in which a plurality of five-transistor cells each including first and second CMOS

inverter circuits having a latch structure and a control transistor, the control transistor being connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line, are connected to a plurality of bit lines and a plurality of word lines, a source voltage commonly applied to a source terminal of an N-type MOS transistor of at least the second CMOS inverter circuit of each of the five-transistor SRAM cells connected to the bit lines can be switched at the "1" data writing time and when it is in another mode (e.g., standby mode, data reading mode, or "0" data write mode). To be more specific, a second voltage which is different from a first voltage (the second voltage is different from the first voltage by predetermined voltage ΔV) is applied at the "1" data writing time, and the first voltage is applied when it is in another mode.

In contrast, Lattimore et al (U.S. Pat. No. 5,831,896) discloses a five-transistor SRAM cell having a latch structure, and Rapp (U.S. Pat. No. 4,189,785) discloses fluctuating a source voltage. However, Applicant respectfully traverses the 35 U.S.C. § 103(a) rejection over these references for the following reasons.

Lattimore et al merely discloses an example of a five-transistor cell having a latch transistor. Moreover, in Lattimore et al, a source voltage of each NFET 104 connected to each other in the word line wire direction is switched (see Figure 1). In other words, in Lattimore et al., the source voltage of the NFET 104 connected to the transfer gate (node on a data-writing side) is switched, which is clearly different in structure from the present invention wherein source voltages of each N-type MOS transistor 22b are connected to each other in the bit line BL direction and are not connected to a transfer gate (connected to the node on the side other than the data-writing side).

On the other hand, Rapp discloses that a source voltage is fluctuated in every mode, such as a reading mode and a wiring mode. Moreover, in Rapp, source terminals of N-channel MOSFET 36 (connected to the node which is not for writing) are connected to each other in the

word line (LINE 26, 30) direction parallel to sense amplifier circuitry 124 (see Figure 1).

Hence, Lattimore et al and Rapp are essentially different from the present invention, and neither reference individually or in combination discloses or suggests the structure of the present invention. Moreover, even if Lattimore et al and Rapp were to be combined, without impermissible hindsight gained from Applicant's disclosure, it is not easy for a person having ordinary skill in the art to obtain the structure of the present invention that a source voltage of each N-type MOS transistor 22b connected in the bit line direction is switched only at the "1" data writing time.

Thus, the configuration of the present invention offers advantages that cannot be obtained from Lattimore et al or Rapp or a combination thereof. Therefore, Applicant submits that the present invention is not made obvious in view of Lattimore et al and Rapp.

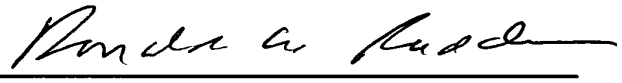
Lastly, Applicant submits that "VSS + ΔV " in original Figure 9 is erroneous, and should have been previously corrected to -- VSS – ΔV --, as was corrected in modified Figure 8 submitted with the last response. As such, the present amendment submits Replacement Figure 9 correcting this designation. Having corrected Figures 8 and 9, the rationale given in the previously filed amendment as to why the previously submitted change to Figure 8 is not new matter holds for Figure 9,[1] and removes the contention raised in the outstanding Office Action that the changes to Figure 8 represent newly added material that is not an obvious error since this change is added for Figure 8 only and Figure 9 still recites VSS + ΔV.[2]

[1] See Remarks on pages 6-8 in the amendment filed November 18, 2004.
[2] Office Action, page 3, lines 11-14.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Customer Number
22850

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Ronald A. Rudder, Ph.D.
Registration No. 45,618

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)
EHK:RAR:clh

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